Statement of Volatility – Dell PowerEdge FM120x4

Dell PowerEdge FM120x4 contains both volatile and non-volatile (NV) components. Volatile components lose their data immediately upon removal of power from the component. Non-volatile components continue to retain their data even after the power has been removed from the component. Components chosen as user-definable configuration options (those not soldered to the motherboard) are not included in the Statement of Volatility. Configuration option information (pertinent to options such as microprocessors, remote access controllers, and storage controllers) is available by component separately. The following NV components are present in the PowerEdge FM120x4 server.

Item	Non-Volatile or Volatile	Quantity	Reference Designator	Size
Planar				
Node Internal CMOS RAM	Non-Volatile	4	Node A: U_CPU1 Node B: U_CPU3 Node C: U_CPU2 Node D: U_CPU4	242 Bytes
Node BIOS SPI Flash	Non-Volatile	4	Node A: U_SPI_BIOS1 Node B: U_SPI_BIOS3 Node C: U_SPI_BIOS2 Node D: U_SPI_BIOS4	8 MB
Node iDRAC SPI Flash	Non-Volatile	4	Node A: U_IDRAC1_SPI Node B: U_IDRAC3_SPI Node C: U_IDRAC2_SPI Node D: U_IDRAC4_SPI	4 MB
Node iDRAC EMMC	Non-Volatile	4	Node A: U_EMMC1 Node B: U_EMMC3 Node C: U_EMMC2 Node D: U_EMMC4	4 GB
Node Network EEPROM	Non-Volatile	4	Node A: U_SPI_LAN1 Node B: U_SPI_LAN3 Node C: U_SPI_LAN2 Node D: U_SPI_LAN4	32 KB
Fabric A Switch EEPROM	Non-Volatile	1	U_5396_SPI	128 Bytes
Fabric D Switch EEPROM	Non-Volatile	1	U_5325E_SPI	128 Bytes
System CPLD RAM	Volatile	1	U_SCPLD	1 KB
Node CPLD RAM	Volatile	1	Node A: U_CPLD1 Node B: U_CPLD3 Node C: U_CPLD2 Node D: U_CPLD4	1 KB
System Memory	Volatile	Up to 2 per Node	Node A: J_DIMM0_CPU1, J_DIMM1_CPU1 Node B: J_DIMM0_CPU3, J_DIMM1_CPU3 Node C: J_DIMM0_CPU2, J_DIMM1_CPU2 Node D: J_DIMM0_CPU4, J_DIMM1_CPU4	Up to 8GB per DIMM

Item	Type (e.g. Flash PROM, EEPROM)	Can user programs or operating system write data to it during normal operation?	Purpose? (e.g. boot code)
Planar			
Node Internal CMOS RAM	Battery-backed CMOS RAM	No	Real-time clock
Node BIOS SPI Flash	SPI Flash	No	Boot code, system configuration information, UEFI environment, Flash Descriptor, ME
Node iDRAC SPI Flash	SPI Flash	No	iDRAC Uboot (bootloader), server management persistent store (i.e. IDRAC MAC Address, iDRAC boot variables), lifecycle log cache, virtual planar FRU and EPPID, rac log, System Event Log,
Node iDRAC EMMC	eMMC NAND Flash	No	Operational iDRAC FW, Lifecycle Controller (LC) USC partition, LC service diags, LC OS drivers, USC firmware
Node Network EEPROM	EEPROM	No	LOM network settings
Fabric A Switch EEPROM	EEPROM	No	FabA switch settings
Fabric D Switch EEPROM	EEPROM	No	FabD switch settings
CPLD RAM	RAM	No	Not utilized
System Memory	RAM	Yes	System OS RAM

Item	How is data input to this memory?	How is this memory write protected?
Planar		
Node Internal CMOS RAM	BIOS	N/A – BIOS only control
Node BIOS SPI Flash	SPI interface via iDRAC	Software write protected
Node iDRAC SPI Flash	SPI interface via iDRAC	Embedded iDRAC subsystem firmware actively controls sub area based write protection as needed.

Item	How is data input to this memory?	How is this memory write protected?
Node iDRAC EMMC	NAND Flash interface via iDRAC	Embedded FW write protected
Node Network EEPROM	SPI interface via CPU nodes	Software Write Protected
Fabric A Switch EEPROM	SPI interface via iDRAC	Software Write Protected
Fabric D Switch EEPROM	SPI interface via iDRAC	N/A- Controlled by the Chassis Management Controller (CMC)
CPLD RAM	Not utilized	Not accessible
System Memory	System OS RAM	System OS
System Memory	System OS	OS Control

NOTE: For any information that you may need, direct your questions to your Dell Marketing contact.